

FIG. 1 is a block diagram of a communication system 100. The system 100 includes a transmitter 102, a channel 120, and a receiver 122. The transmitter 102 includes an encoder 106, an interleaver 108, a bit to symbol mapper 110, a modulator 112, and a Tx block 114. The receiver 122 includes an Rx front end 124, an inner decoder (equalizer) 126, a de-interleaver 128, and an outer decoder 130. The channel 120 is between the transmitter 102 and the receiver 122. The transmitter 102 receives transmit data 104 and outputs a signal s(k) to the channel 120. The receiver 122 receives a signal x(k) from the channel 120 and outputs receive data 138.

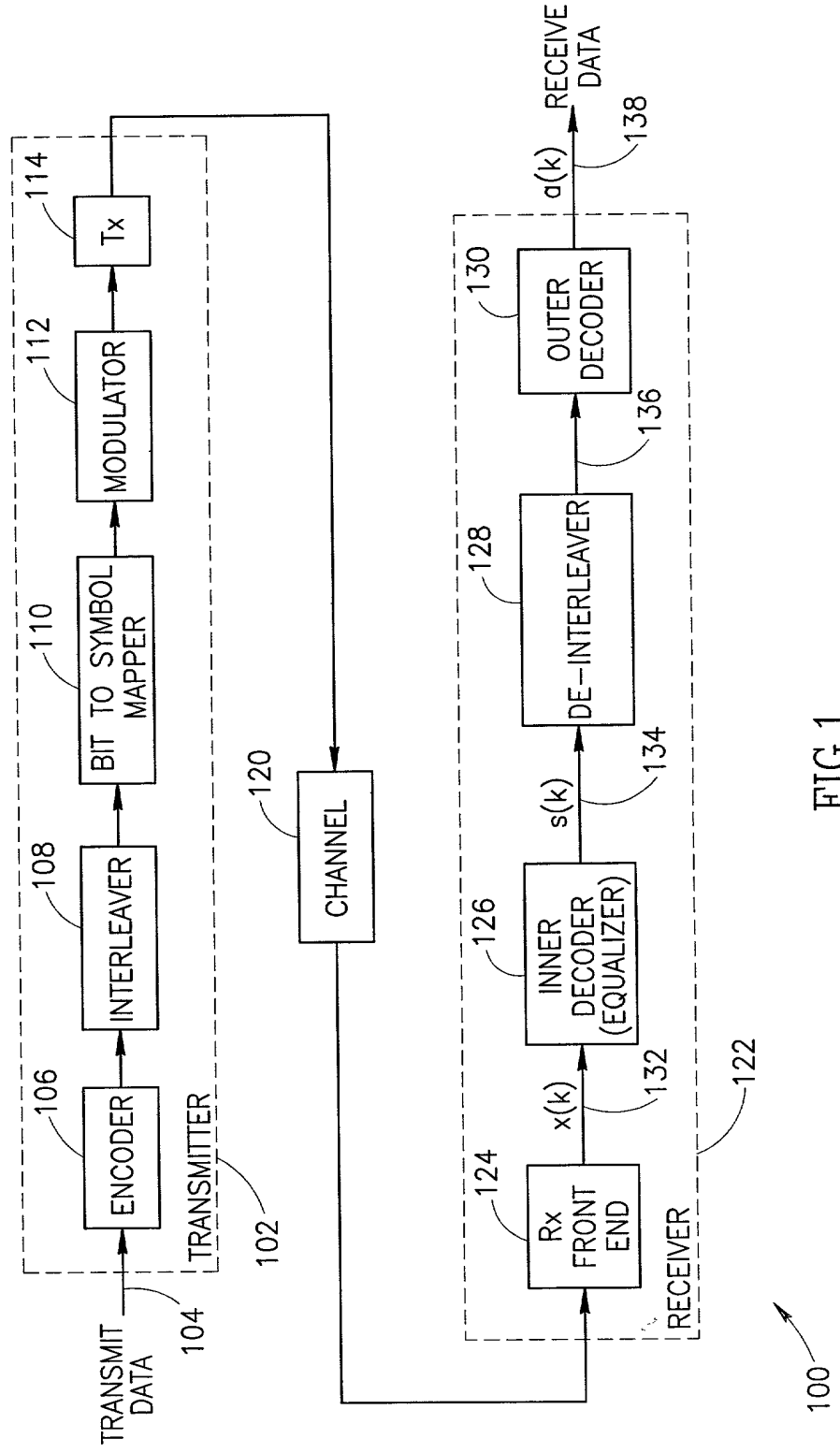


FIG.1

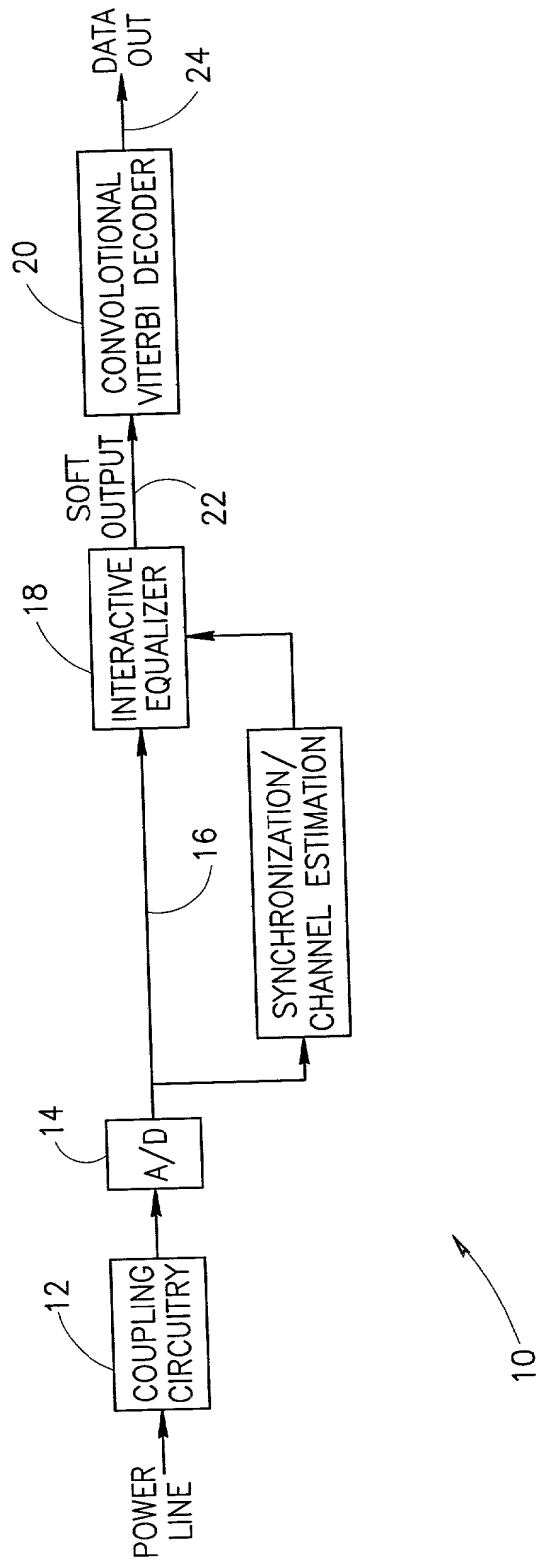


FIG.2

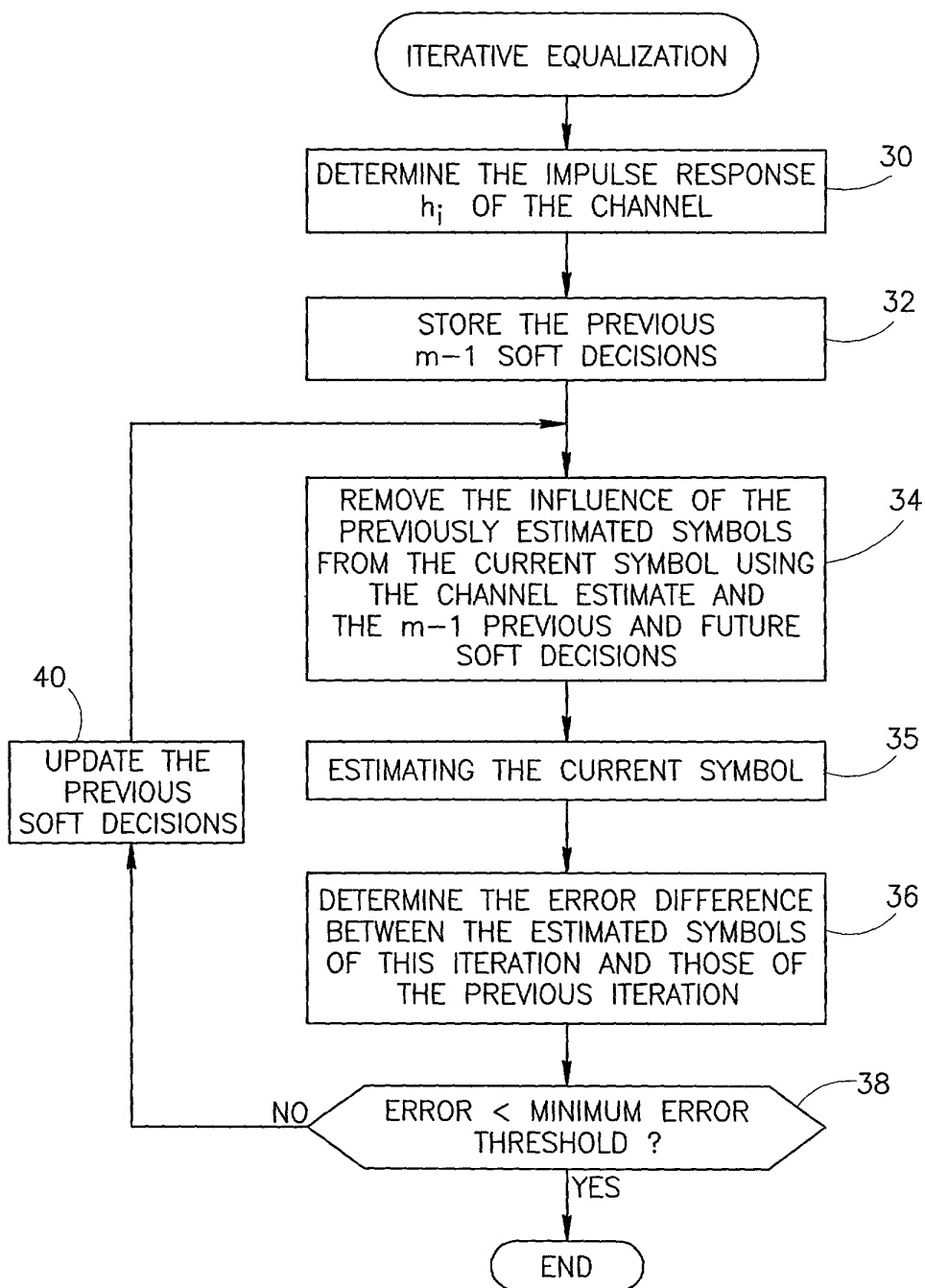
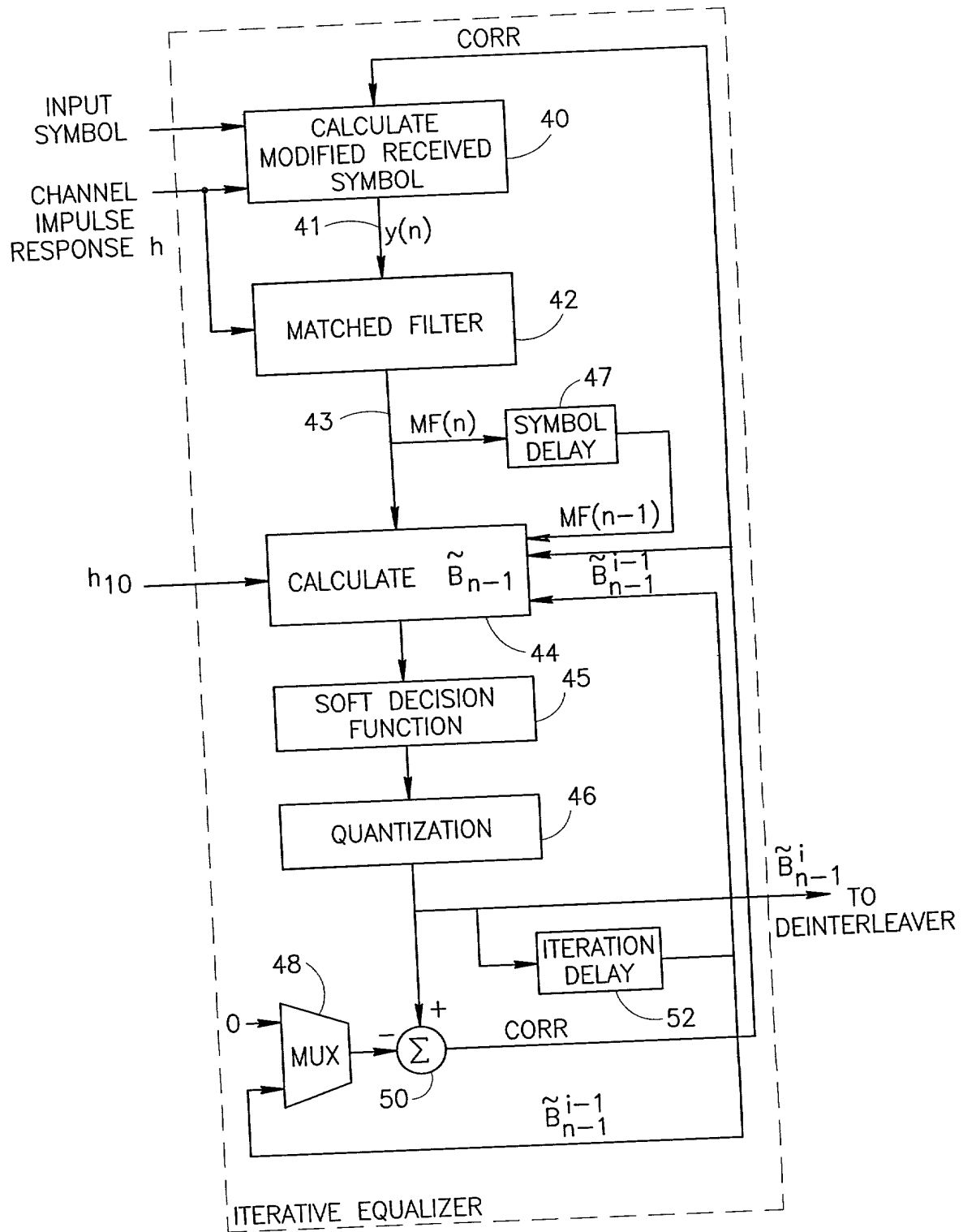


FIG.3



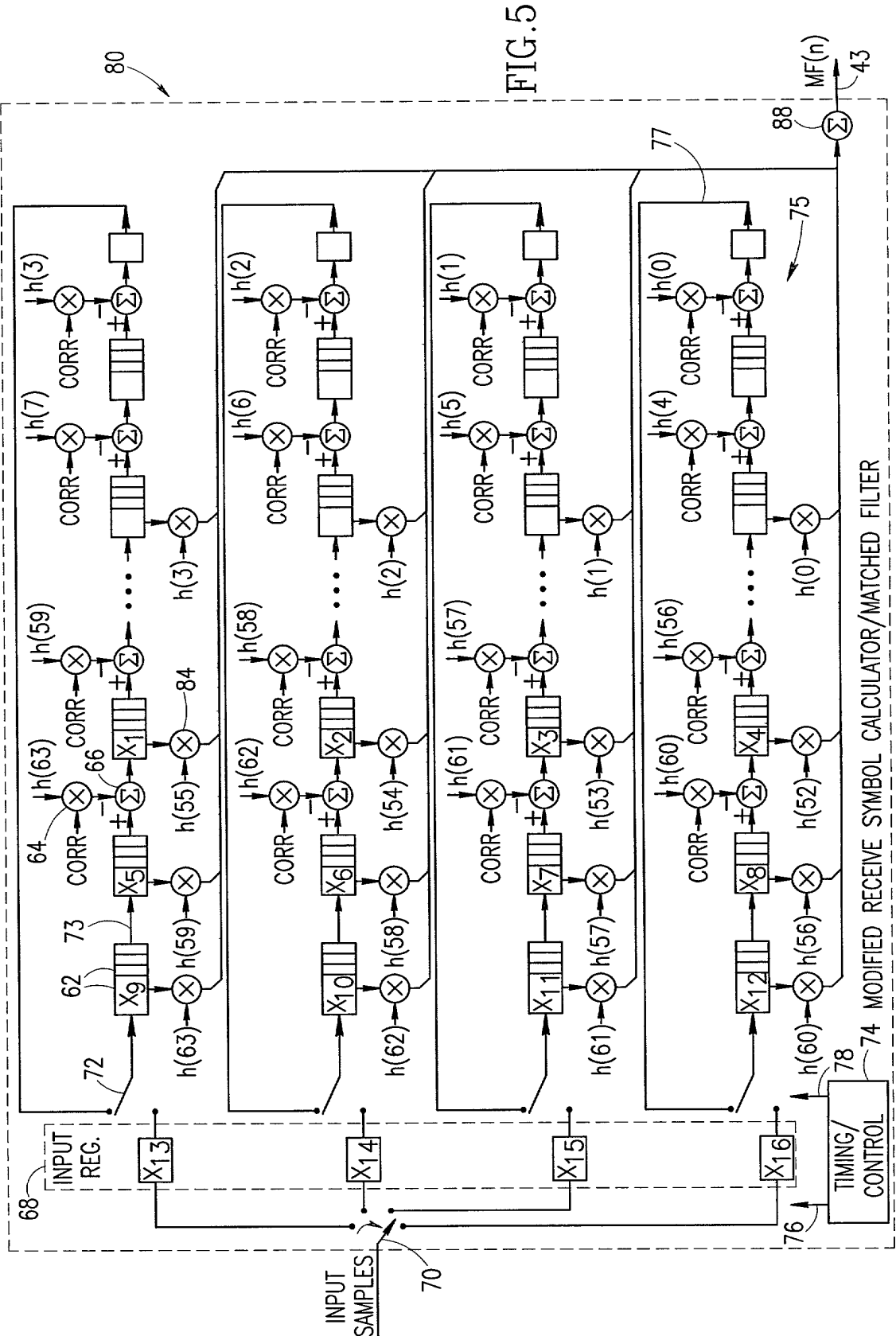


FIG. 5

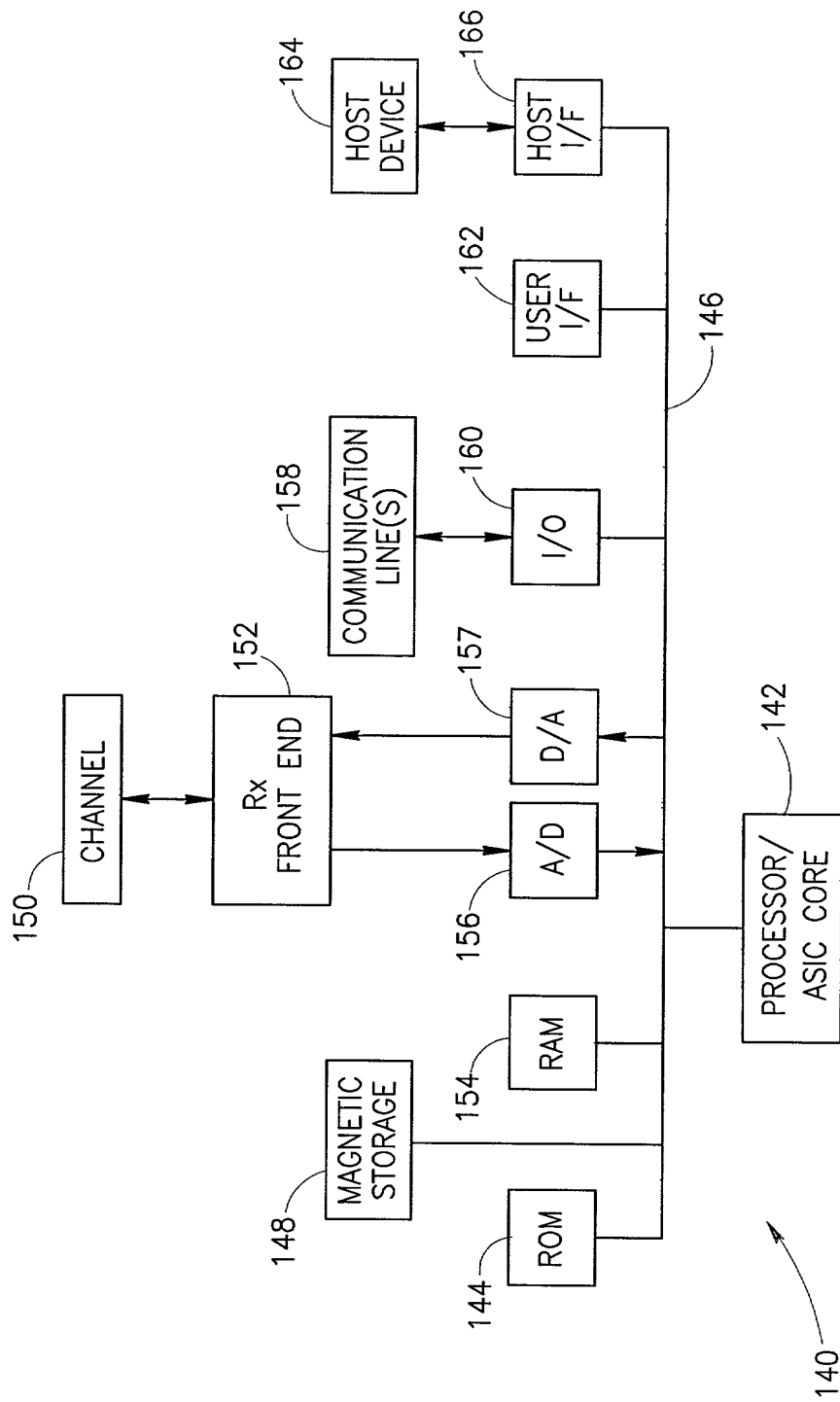


FIG. 6